implanting a well region at least partially within the vertical fin-shaped structure to be a first doping polarity; and

implanting a buffer region in the vertical fin-shaped structure to be a second doping polarity which is opposite to the first doping polarity,

wherein at least one p-n junction is formed between the buffer region and the well region and at least partially covers a horizontal cross section of the vertical fin-shaped structure,

wherein the buffer region is implanted within the well region, such that a first p-n junction is formed between the buffer region and a first layer of the well region, and a second p-n junction is formed between the buffer region and a second layer of the well region.

9. The method of claim **8**, further comprising:

performing a trench etch to form trenches defining side surfaces of the vertical fin-shaped structure; and

filling the trenches with oxide.

10. The method of claim **9**, wherein the trench etch also forms trenches defining side surfaces of a vertical well-tap structure which bypasses the buffered vertical fin-shaped structure and electrically connects to the well region.

11. The method of claim **9**, further comprising:

performing an oxide recess such that the oxide in the trenches is recessed so as to expose an upper semiconductor layer of the vertical fin-shaped structure.

12. The method of claim **11**, further comprising:

forming a gate stack over a channel region of the upper semiconductor layer.

13. The method of claim **12**, further comprising:

forming gate stack spacers adjacent to the gate stack; and

performing selective epitaxial growth on source and drain regions of the upper semiconductor layer.

14. The method of claim **8**, wherein the buffer region is implanted directly above the well region, such that one p-n junction is formed between the buffer region and the well region.

15. The method of claim **8**, wherein implants of the well and buffer regions are such that the horizontal cross section of the vertical fin-shaped structure is fully covered by the at least one p-n junction.

16. An integrated circuit comprising at least one buffered finFET device, the buffered finFET device comprising:

a buffered vertical fin-shaped structure which includes at least

an upper semiconductor layer including a channel region in between drain and source regions,

a buffer region beneath the upper semiconductor layer, the buffer region having a first doping polarity,

at least part of a well region having a second doping polarity which is opposite to the first doping polarity, and

at least one p-n junction between the buffer region and the well region which at least partially covers a horizontal cross section of the vertical fin-shaped structure; and

a gate stack formed over the channel region of the upper semiconductor layer,

wherein a first layer of the well region is directly above the buffer region, and a second layer of the well region is directly below the buffer region at the base of the buffered vertical fin-shaped structure, such that two p-n junctions are present between the buffer region and the well region.

17. The integrated circuit of claim **16**, further comprising:

a well tap which bypasses the buffered vertical fin-shaped structure and electrically connects to the well region.

18. The integrated circuit of claim **16**, wherein the buffered finFET device is part of a static memory cell.

19. The integrated circuit of claim **16**, wherein the buffered finFET device is part of an analog circuit.

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